REMARKS/ARGUMENTS

Examiner Isaac is thanked for the continued thorough Search and Examination of the Subject Application for Patent. Examiner Isaac is also thanked for withdrawing the finality of the rejections of the previous Office Action.

Reconsideration of the Rejection of Claims 1-19 under 35 U.S.C. 103(a) as being unpatentable over Stanley Wolf, Vol. II, (Silicon Processing for the VLSI Era, Vol. II, Process Integration, Lattice Press, 1990) in view of Lin (U.S. Pat. No. 6,524,950) in view of Detzel et al. (U.S. Pat. No. 6,287,174) is requested. Claims 1-19 describe methods of planarizing substrates having trenches formed therein. A layer of dielectric is formed on the substrate thereby filling the trenches with the dielectric. A layer of resist is then formed on the layer of dielectric. The substrate is then planarized by removing all of the layer of resist and part of the layer of dielectric using only chemical mechanical polishing with a hard polishing pad, a hardness of at least Shore "D" 52. Key limitations of the methods of Claims 1-19 are "forming a layer of resist on said layer of trench dielectric; providing a polishing pad having a hardness of at least Shore "D" 52; and removing all of said layer of resist and part of said layer of trench dielectric using said polishing pad and chemical mechanical polishing". A polishing pad with a hardness of at least Shore "D" 52 is used to remove the combined layer of resist and dielectric. Using a polishing pad with a hardness of at least Shore "D" 52 is an important part of Claims 1-19 because this insures that the layer of resist and dielectric is removed without leaving scratch marks on the remaining trench dielectric, any base dielectric on the surface of the

substrate, or on the surface of the substrate if there is no base dielectric on the substrate, see the Specification page 9, lines 9-17 and page 11, lines 8-15. Softer polishing pads will leave scratch marks when used to remove a layer of resist and dielectric.

The Examiner has argued that Stanley Wolf, Vol. II, (Silicon Processing for the VLSI Era, Vol. II, Process Integration, Lattice Press, 1990), hereinafter referred to as Wolf, in Fig. 2-31 describes the methods of Claims 1 and 11 except that Wolf fails to describe the step of chemical mechanical polishing. We respectfully disagree. In Fig. 2-31 Wolf describes a method of planarizing substrates using an RIE etchback technique. The RIE etchback technique is very different from the chemical mechanical polishing described in Claims 1-19. It is not obvious from the RIE etchback described by Wolf that that chemical mechanical polishing using a polishing pad having a hardness of at least Shore "D" 52, as described in Claims 1-19, can be substituted for the RIE etchback to remove all of the layer of resist and part of the layer of trench dielectric. As indicated in the Specification page 9, lines 9-17 and page 11, lines 8-15 the methods of Claims 1-19 are used to avoid scratch marks on the remaining trench dielectric when using chemical mechanical polishing to remove the layer of resist and part of the trench dielectric.

Lin describes a method of fabricating a copper damascene structure. As indicated by the Examiner, Lin describes the use of chemical mechanical polishing as part of the method. However, it is believed that Lin does not make the methods described by Claims 1-19 an obvious extension of Wolf because the RIE etchback technique described by Wolf, which utilizes chemical etching of material, is significantly

different from chemical mechanical polishing, which removes material substantially by abrasion. Chemical mechanical polishing is significantly different from RIE etchback and it is not obvious to substitute the chemical mechanical polishing described by Lin for the RIE etchback described by Wolf. As is also indicated by the Examiner, Lin does not describe chemical mechanical polishing using a polishing pad having a specific hardness, as is described in Claims 1-19.

Detzel et al. describe a polishing pad for semiconductor wafers and a method of disengaging the wafer from the polishing pad after polishing, see the Abstract. Detzel et al. describe a number of properties for a preferred pad and included in the list of properties is "a hardness of 25 to 80 Shore D", see column 4, line 22. The methods of Claims 1-19 specify a polishing pad having a hardness of at least Shore "D" 52 in order to prevent leaving scratch marks on the remaining trench dielectric, any base dielectric on the surface of the substrate, or on the surface of the substrate if there is no base dielectric on the substrate. Greater than 49% of the hardness range described by Detzel et al. do not meet the criterion of having a hardness of at least Shore "D" 52 and would not work as intended in Claims 1-19. In addition Claims 1-19 do not put an upper limit on the hardness of the polishing pad.

We wish to emphasize that the Specification on page 9, lines 9-15 recites "One of the key features of this invention is that the polishing pad 32 is very hard having a hardness of at least Shore "D" 52. This hard polishing pad planarizes the wafer without leaving scratch marks on the remaining trench dielectric 18, any base dielectric 11 on the

surface of the substrate 10, or the surface of the substrate 10 if there is no base dielectric 11 used on the substrate 10." The Specification on page 11, lines 8-13 further recites "In this embodiment, as in the preceding embodiment, a key to the invention is that the polishing pad 32, see Fig. 6, is very hard having a hardness of at least Shore "D" 52. This hard polishing pad planarizes the wafer without leaving scratch marks on the remaining trench dielectric 18 or on the surface of the substrate 10."

It is believed that Claims 1-19 are different from and not obvious from Wolf in view of Lin in view of Detzel et al. because of the key limitations of Claims 1-19 of "forming a layer of resist on said layer of trench dielectric; providing a polishing pad having a hardness of at least Shore "D" 52; and removing all of said layer of resist and part of said layer of trench dielectric using said polishing pad and chemical mechanical polishing". Wolf describes using RIE etchback to remove resist and dielectric material. Lin describes chemical mechanical polishing but does not make using chemical mechanical polishing to remove resist and trench dielectric obvious from Wolf because the removal techniques of RIE etchback and chemical mechanical polishing are entirely different and it is not obvious to substitute chemical mechanical polishing for the RIE etchback described by Wolf. Detzel et al. describe a polishing pad having a hardness of 25 to 80 Shore D but do not make a polishing pad having a hardness of at least Shore "D" 52 as is specified in Claims 1-19 an obvious extension of Wolf and Lin. Claims 1-19 do not specify an upper limit on the hardness of the polishing pad and more than 49% of the hardness range specified by Detzel et al. do not meet the limitations of Claims 1-19. Reconsideration of the Rejection of Claims 1-19 under 35 U.S.C. 103(a) as being

unpatentable over Wolf in view of Lin in view of Detzel et al., and allowance of Claims 1-19, are requested.

It is requested that should Examiner Isaac not find that the Claims are now Allowable that the Examiner call the undersigned Agent at (845)-462-5363 to overcome any problems preventing allowance.

Respectfully submitted,

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